Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Ex parte LARRIE CARR

Appeal No. 2003-1091
Application No. 09/484,248

ON BRIEF

Before THOMAS, RUGGIERO, and LEVY, Administrative Patent Judges.

RUGGIERO, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on the appeal from the final rejection of claims 1-20, which are all of the claims pending in the present application.

The claimed invention relates to a digital delay line which includes a plurality of multiplexer delay elements each having a control input which transmits a control signal to each multiplexer. Further included in the digital delay line is a

clock signal line, coupled to a clock input on each multiplexer, which provides synchronous phase aligned clock signals to each clock input from a clock signal source. In response to changes in the control signal, associated delay elements are removed or added to the delay line in single step.

Claim 1 is illustrative of the invention and reads as follows:

1. A digital delay line, comprising:
   (a) a plurality of multiplexer delay elements arranged in sequence each of said plurality of multiplexer delay elements having an associated control input;
   (b) a clock signal line coupled to a clock input of each of said plurality of multiplexers, said clock signal line operative to provide synchronous phase aligned clock signals from a clock signal source to each of said clock inputs; and
   (c) a control input coupled to each of said plurality of multiplexer delay elements operative to transmit to each of said plurality of multiplexer delay elements an associated control signal and, in response to said control signal, to select or deselect, in a single step, up to a plurality of delay elements from a start of said delay line.

The Examiner relies on the following prior art references:[1]

Butcher	4,789,996	Dec. 06, 1988
Takano et al. (Takano)	5,940,414	Aug. 17, 1999

Claims 1 and 14 stand finally rejected under 35 U.S.C. § 102(b) as being anticipated by Butcher. Claims 2-13 and 15-20

[1] In addition, the Examiner relies on Appellant's admissions as to a prior art clocking structure illustrated at Figure 1 in Appellant's drawings.

stand finally rejected under 35 U.S.C. § 103(a). As evidence of obviousness, the Examiner offers Butcher in view of Takano with respect to claims 2-8, 11-13, and 15-20, and Butcher in view of the admitted prior art with respect to claims 9 and 10.[2]

Rather than reiterate the arguments of Appellant and the Examiner, reference is made to the Briefs[3] and the Answer for the respective details.

OPINION

We have carefully considered the subject matter on appeal, the rejections advanced by the Examiner, and the evidence of anticipation and obviousness relied upon by the Examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, Appellant's arguments set forth in the Briefs along with the Examiner's rationale in support of the rejections and arguments in rebuttal set forth in the Examiner's Answer.

It is our view, after consideration of the record before us, that the disclosure of Butcher fully meets the invention as

[2] As indicated at page 2 of the Answer, the Examiner has withdrawn the rejections under the first and second paragraphs of 35 U.S.C. § 112.

[3] The Appeal Brief was filed September 13, 2002 (Paper No. 16). In response to the Examiner's Answer dated December 3, 2002 (Paper No. 18), a Reply Brief was filed February 3, 2003 (Paper No. 19) which was acknowledged and entered by the Examiner as indicated in the communication dated March 20, 2003 (Paper No. 20).

recited in claims 1. We reach the opposite conclusion with respect to claim 14. In addition, we are of the opinion that the evidence relied upon and the level of skill in the particular art would have suggested to one of ordinary skill in the art the obviousness of the invention set forth in claims 2-13 and 18-20, but not the invention as recited in claims 15-17. Accordingly, we affirm-in-part.

We consider first the Examiner's 35 U.S.C. § 102(b) rejection of claims 1 and 14 based on Butcher. At the outset, we note that anticipation is established only when a single prior art reference discloses, expressly or under the principles of inherency, each and every element of a claimed invention as well as disclosing structure which is capable of performing the recited functional limitations. RCA Corp. v. Applied Digital Data Systems, Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir.); cert. dismissed, 468 U.S. 1228 (1984); W.L. Gore and Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984).

With respect to independent claim 1, the Examiner indicates (Answer, pages 3 and 4) how the various limitations are read on the disclosure of Butcher. In particular, the Examiner directs attention to the illustration in Figure 3 of Butcher along with

the accompanying description beginning at column 5, line 32.

After reviewing the Examiner's analysis, it is our opinion that the stated position is sufficiently reasonable that we find that the Examiner has at least satisfied the burden of presenting a prima facie case of anticipation. The burden is, therefore, upon Appellant to come forward with evidence and/or arguments which persuasively rebut the Examiner's prima facie case. Only those arguments actually made by Appellant have been considered in this decision. Arguments which Appellant could have made but chose not to make in the Briefs have not been considered [see 37 CFR § 1.192(a)].

Appellant's argument in response (Brief, pages 7 and 8; Reply Brief, pages 5-7) to the Examiner's anticipation rejection asserts that the Examiner has misinterpreted the disclosure of Butcher. In particular, Appellant contends that since the shift register 11 in Butcher, which determines the number of gate delay elements in delay line 10, operates by shifting a value one step in one direction at a time, Butcher " . . . cannot de(select) a plurality of delay elements in a single step as claimed . . . ." (Brief, at 8).

After careful review of the Butcher reference in light of

the arguments of record, we are in agreement with the Examiner's position as stated in the Answer. Our review of the arguments of record reveals that Appellant and the Examiner are in general agreement as to the operation of the device of Butcher, i.e., each value shift of shift register 11 adds or removes a delay element. We also do not disagree with Appellant that the operation of Butcher differs from that disclosed by Appellant in which the change of a single bit in a clock line pattern results the selection or removal of plural delay elements in a delay line. It is the claimed invention, however, which is at issue before us, and we find that Appellant's arguments are not commensurate with the scope of the actual language of claim 1. In contrast to Appellant's arguments that claim 1 requires the single step selection of a plurality of delay elements, the actual language of claim 1 recites the selection of " . . . up to a plurality of delay elements . . . ." In our view, this claim language clearly encompasses the selection in a single step of a single delay element, a feature which even Appellant has recognized is disclosed by Butcher. Appellant's arguments improperly attempt to narrow the scope of the claim by implicitly adding disclosed limitations which have no basis in the claim. See In re Morris, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28

(Fed. Cir. 1997).

In view of the above discussion, since all of the claimed limitations are present in the disclosure of Butcher, the Examiner's 35 U.S.C. § 102(b) rejection of claim 1 is sustained.

Turning to a consideration of the Examiner's 35 U.S.C. § 102(b) rejection of claim 14 based on Butcher, we note that, while we found Appellant's arguments to be unpersuasive with respect to the anticipation rejection of claim 1, we reach the opposite conclusion with respect to claim 14. In contrast to the previously discussed language of claim 1 which requires only the single step selection of " . . . up to a plurality of delay elements . . .," the language of claim 14 clearly and unambiguously recites the single step selection (or deselection) of " . . . two or more elements . . . ."

Our interpretation of the disclosure of Butcher coincides with that of Appellant, i.e., while the end result of a value shift in Butcher's shift register 11 may be the addition or removal of a delay element to an existing plurality of delay elements as suggested by the Examiner (Answer, page 4), the resulting plural delay elements have not been selected or deselected in a single step. We further agree with Appellant (Reply Brief, page 5) that, in order for Butcher's described

operation to approximate the language of appealed claim 14, all currently selected delay elements would have to be deselected, a value shift performed in the shift register, followed by a selection of the newly selected elements, an operation not supported by the disclosure of Butcher. Accordingly, since all of the limitations of claim 14 are not present in the disclosure of Butcher, the Examiner's 35 U.S.C. § 102(b) rejection of claim 14 is not sustained.

We also do not sustain the Examiner's 35 U.S.C. § 103(a) rejection of claims 15-17, dependent on claim 14, in which the Takano reference is added to Butcher to address the logic gate details of these claims. We find nothing, however, in Takano which would overcome the innate deficiency of Butcher in disclosing the single step selection of a plurality of delay elements as discussed supra.

We do, however, sustain the Examiner's 35 U.S.C. § 103(a) rejections of claims 2-8, 11-13, and 18-20 based on the combination of Butcher and Takano, and of claims 9 and 10 based on the combination of Butcher and the admitted prior art. Our review of the Examiner's analysis at pages 5-8 of the Answer reveals no error in the Examiner's position. Appellant's arguments in the principal Brief with respect to these claims

rely on assertions made with respect to claim 1, i.e., that Butcher fails to disclose the single step selection of a plurality of delay elements. As previously discussed, we find these arguments unpersuasive since the language of claim 1 does not require the selection of a plurality of delay elements but, rather, only the single step selection of "up to a plurality of delay elements." Since Appellant, by the presented arguments, has chosen to let the rejection of claims 2-8, 11-13, and 18-20 stand or fall with claim 1, the Examiner's 35 U.S.C. § 103(a) rejection of these claims is sustained. Note In re King, 801 F.2d 1324, 1325, 231 USPQ 136, 137 (Fed. Cir. 1986); In re Sernaker, 702 F.2d 989, 991, 217 USPQ 1, 3 (Fed. Cir. 1983).

We have taken note of Appellant's presentation, for the first time, in the Reply Brief of arguments directed to claims 2 and 20, as well as the discussion of features of other unspecified claims. We will not consider these new arguments. Because an Examiner is no longer permitted to file sua sponte a supplemental Examiner's Answer in response to a Reply Brief, 37 CFR § 1.193(b)(1)(1998), we do not have the benefit of the Examiner's response to Appellant's new arguments. Considering the new arguments would not only be unfair but would entail the risk of an improvident or ill-advised opinion. Cf. Kaufman Co. v

Lantech Inc., 807 F.2d 970, 973 n.*, 1 USPQ2d 1202, 1204 n.* (Fed. Cir. 1986).

In summary, with respect to the Examiner's 35 U.S.C. § 102(b) rejection, we have sustained the rejection of claim 1, but have not sustained the rejection of claim 14. We have also sustained the Examiner's 35 U.S.C. § 103(a) rejection of claims 2-13 and 18-20, but have not sustained the 35 U.S.C. § 103(a) rejection of claims 15-17. Therefore, the Examiner's decision rejecting claims 1-20 is affirmed-in-part.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

James D. Thomas Administrative Patent Judge	)
Joseph F. Ruggiero Administrative Patent Judge	) BOARD OF PATENT) APPEALS AND) INTERFERENCES
Stuart S. Levy Administrative Patent Judge	)

JFR/eld

Hall, Priddy & Myers
10220 River Road
Suite 200
Potomac, MD 20854